UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/098,694	03/12/2002	Laurence B. Boucher	ALA-009C	7052

			EXAMINER
24501	7590	02/06/2006	KUIPER, ERIC J

MARK A LAUER
6601 KOLL CENTER PARKWAY
SUITE 245
PLEASANTON, CA 94566

ART UNIT	PAPER NUMBER
2154	

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Please find below and/or attached an Office communication concerning this application or proceeding.

	Application No.	Applicant(s)
Office Action Summary	10/098,694	BOUCHER ET AL.
	Examiner	Art Unit	
	Eric Kuiper	2154	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on <u>12 March 2002</u>.

2a) ☐ This action is **FINAL**.   2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *1-20* is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) *1-20* is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a) ☐ All   b) ☐ Some * c) ☐ None of:

      1. ☐ Certified copies of the priority documents have been received.

      2. ☐ Certified copies of the priority documents have been received in Application No. _____.

      3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____ .

DETAILED ACTION

1.   Claims 1-20 have been presented for examination.

Claim Rejections - 35 USC § 103

2.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in
> section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are
> such that the subject matter as a whole would have been obvious at the time the invention was made to a person
> having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the
> manner in which the invention was made.

3.   The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459

(1966), that are applied for establishing a background for determining obviousness under 35

U.S.C. 103(a) are summarized as follows:

1.   Determining the scope and contents of the prior art.
2.   Ascertaining the differences between the prior art and the claims at issue.
3.   Resolving the level of ordinary skill in the pertinent art.
4.   Considering objective evidence present in the application indicating obviousness
        or nonobviousness.

4.   Claims 1-6, and 8-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over

Mayer et al. (US 6,233,242, hereinafter Mayer) in view of Kapoor et al. (US 5,682,534,

hereinafter Kapoor).

5.   As per claim 1, Mayer teaches a method comprising:

maintaining a set of communication control blocks (CCBs), some of the set of CCBs

being maintained in a static random access memory (SRAM), others of the set of CCBs being

maintained in a dynamic random access memory (DRAM), wherein a first plurality of the set of

CCBs is under control of a network interface device, and wherein a second plurality of the set of

CCBs is under control of a processing device, the processing device being coupled to the

network interface deice, the processing device executing a network protocol stack (e.g. Mayer,

several types of "control blocks" are disclosed, high speed bus control block, memory control

block, processor control block, all relating to communication procedures also the maintaining of

the control blocks in both DRAM and SRAM, col. 17, lines 11-17, 25-31; col. 31, lines 63-67;

col. 32, lines 1-30);

receiving a packet onto the network interface device from a network, the packet including

a data portion and a header portion (e.g. Mayer, col. 7, lines 52-67);

using content addressable memory (CAM) on the network interface device to determine

that the packet is associated with one of the first plurality of CCBs (e.g. Mayer, CAM is taught

as an alternative form of SRAM, similar in both use and function, col. 2, lines 28-35; col. 58,

lines 44-51);

determining on the network interface device that said one CCB is stored in the DRAM

and transferring said one CCB into the SRAM (e.g. Mayer, col. 31, lines 63-67; col. 32, lines 1-

30); and

transferring the data portion of the packet from the network interface device into a

destination without transferring the header portion of the packet into the destination, the

destination having been determined by the processing device (e.g. Mayer, col. 15, lines 46-52).

Mayer fails to teach the method wherein the packet is a TCP/IP packet and wherein the

network protocol stack executing on the processing device performs substantially no TCP

protocol processing on the TCP/IP packet.

However, in a similar art, Kapoor teaches a network communications device which operates on TCP/IP packets using a network protocol stack (e.g. Kapoor, col. 3, lines 49-51) and also the ability to avoid, or bypass, the processing of a packet on the TCP (transport) layer of the protocol stack (e.g. Kapoor, col. 2, lines 33-49; col. 6, lines 7-19; Fig. 2B).

It would have been obvious to one skilled in the art at the time the invention was made to combine Kapoor with Mayer because of the advantages of allowing a packet to avoid processing in various layers of a protocol stack. Kapoor teaches that bypassing the transport layer "provides significant performance gains" for the transmission of packets through the network (e.g. Kapoor, col. 2, lines 44-49). These performance gains include increases in both speed and efficiency of packet transmission, since unnecessary processing is avoided and the packet can be transferred directly to its intended destination. The processor on the network communication device performs the processing that is needed on the packet, thereby allowing the central processing unit of the host, or main computer, to perform other tasks, further increasing the speed and efficiency of packet transmission, which is beneficial to any computer network.

6.   As per claim 2, Mayer and Kapoor teach the method of claim 1, further comprising:

        receiving a second TCP/IP packet (e.g. Kapoor, col. 3, lines 49-51) onto the network interface device from the network (e.g. Mayer, col. 7, lines 52-67);

        determining that the second TCP/IP packet is not associated with any one of the first plurality of CCBs (e.g. Mayer, col. 17, lines 11-17, 25-31); and

        transferring the second TCP/IP packet from the network interface device and to the processing device, the processing device thereafter performing TCP protocol processing on the

second TCP/IP packet (e.g. Kapoor, processing the packet through the entire protocol stack when

it does not meet the requirements for the shortened protocol stack, col. 5, lines 36-45).

7.   As per claim 3, Mayer and Kapoor teach the method of claim 1, wherein the TCP/IP

packet has a TCP destination port, a TCP source port, an IP destination address, and an IP source

address (e.g. Mayer, col. 58, lines 35-44), the method further comprising:

    generating a context hash from the TCP source and destination ports and from the IP

source and destination addresses, the network interface device using the context hash to identify

said one CCB associated with the TCP/IP packet (e.g. Mayer, col. 58, lines 44-51).

8.   As per claim 4, Mayer and Kapoor teach the method of claim 1, wherein control of a

CCB can be passed from the network interface device to the processing device (e.g. Mayer,

memories can be controlled by CPU or ASIC on device, col. 107, lines 20-33).

9.   As per claim 5, Mayer and Kapoor teach the method of claim 1, wherein control of a

CCB can be passed from the processing device to the network interface device (e.g. Mayer, col.

107, lines 20-33).

10.   As per claim 6, Mayer and Kapoor teach the method of claim 1, wherein the network

interface device comprises specialized hardware for generating a hash from the header portion of

the TCP/IP packet, and wherein the network interface device further comprises a processor, the

processor accessing the hash and using the hash to determine that the TCP/IP packet is

associated with said one of the first plurality of CCBs (e.g. Mayer, col. 3, lines 21-30; col. 19, lines 53-67).

11.   As per claim 8, Mayer and Kapoor teach the method of claim 1, wherein the network interface device comprises specialized hardware for generating a summary, and wherein the network interface device further comprises a processor, the processor accessing the summary and using the summary to determine that the TCP/IP packet is associated with said one of the first plurality of CCBs (e.g. Mayer, col. 24, lines 40-62).

12.   As per claim 9, Mayer and Kapoor teach the method of claim 8, wherein the summary includes a hash (e.g. Mayer, col. 24, lines 40-62).

13.   As per claim 10, Mayer and Kapoor teach the method of claim 8, wherein the summary includes information indicative of whether the TCP/IP packet employs both the TCP protocol and the IP protocol (e.g. Mayer, col. 24, lines 40-62; Kapoor, col. 3, lines 49-51).

14.   As per claim 11, Mayer and Kapoor teach the method of claim 1, wherein the processing device is a central processing unit (CPU), and wherein the network interface device is integrated with the CPU (e.g. Mayer, col. 2, lines 11-28).

15.   As per claim 12, Mayer and Kapoor teach the method of claim 1, wherein the processing

device is a host, and wherein the network interface device is integrated into the host (e.g. Mayer,

col. 2, lines 11-28).

16.   As per claim 13, Mayer and Kapoor teach the method of claim 1, wherein the processing

device is a central processing unit (CPU, the network interface device being integrated with the

CPU, and wherein the network interface device comprises a plurality of processors, the plurality

of processors sharing the first plurality of CCBs (e.g. Mayer, col. 2, lines 11-28; col. 107, lines

20-33).

17.   As per claim 14, Mayer teaches a network interface device that is coupled to a processing

device, the processing device executing a protocol stack, the network interface device

comprising:

        an amount of SRAM, the SRAM storing a first plurality of communication control blocks

(CCBs) that are under control of the network interface device (e.g. Mayer, col. 17, lines 11-17;

col. 31, lines 63-67; col. 32, lines 1-30);

        an amount of DRAM, the DRAM storing a second plurality of CCBs that are under

control of the network interface device (e.g. Mayer, col. 17, lines 11-17; col. 31, lines 63-67; col.

32, lines 1-30);

        specialized hardware that analyzes a packet received onto the network interface device

from a network, the packet comprising a data portion and a header portion, the specialized

hardware generating a summary from the packet (e.g. Mayer, col. 7, lines 52-67; col. 3, lines 21-30; col. 19, lines 53-67);

a processor that uses the summary and a content addressable memory (e.g. Mayer, col. 2, lines 28-35; col. 58, lines 44-51), the packet being associated with one of the second plurality of CCBs, the processor causing said one of the second plurality of CCBs to be moved from the DRAM into the SRAM (e.g. Mayer, col. 31, lines 63-67; col. 32, lines 1-30); and

a mechanism that moves the data portion of the packet from the network interface device and into a destination identified by the processing device, the data portion of the packet being written into the destination without the header portion of the packet being written into the destination (e.g. Mayer, col. 15, lines 46-52).

Mayer fails to teach the network interface device wherein the packet is a TCP/IP packet and using the summary to determine whether the TCP/IP packet can be processed via a fast-path by the network interface device as opposed to being processed via a slow-path using the protocol stack, the data portion of the TCP/IP packet being written into the destination without the protocol stack doing substantial TCP protocol processing on the TCP/IP packet.

However, in a similar art, Kapoor teaches a network communications device which operates on TCP/IP packets using a network protocol stack (e.g. Kapoor, col. 3, lines 49-51) and also the ability to avoid, or bypass, the processing of a packet on the TCP (transport) layer of the protocol stack, and if the packet does not meet the requirements for fast processing, performing processing at each layer of the protocol stack (e.g. Kapoor, col. 2, lines 33-49; col. 6, lines 7-19; Fig. 2B; col. 5, lines 36-45).

It would have been obvious to one skilled in the art at the time the invention was made to

combine Kapoor with Mayer for similar reasons as stated above in regards to claim 1.

18.   As per claim 15, Mayer and Kapoor teach the network interface device of claim 14,

wherein the specialized hardware generates from the TCP/IP packet a has, the hash being part of

the summary, the summary being used by the processor to make the determination that the

packet can be processed via the fast-path (e.g. Mayer, col. 3, lines 21-30; col. 19, lines 53-67).

19.   As per claim 16, Mayer and Kapoor teach the network interface device of claim 14,

wherein the summary includes information indicative of whether the TCP/IP packet conforms to

both the TCP protocol and the IP protocol (e.g. Kapoor, col. 3, lines 49-51).

20.   As per claim 17, Mayer teaches a network interface device that is integrated with a

processing device, the processing device executing a protocol stack, the network interface device

comprising:

        an amount of SRAM, the SRAM storing a first plurality of communication control blocks

(CCBs) that are under control of the network interface device (e.g. Mayer, col. 17, lines 11-17;

col. 31, lines 63-67; col. 32, lines 1-30);

        an amount of DRAM, the DRAM storing a second plurality of CCBs that are under

control of the network interface device (e.g. Mayer, col. 17, lines 11-17; col. 31, lines 63-67; col.

32, lines 1-30);

means for analyzing a packet received onto the network interface device from a network

and for generating from the packet a summary, the packet comprising a data portion and a header

portion (e.g. Mayer, col. 7, lines 52-67; col. 3, lines 21-30; col. 19, lines 63-67), the header

portion including a destination port value and a source port value (e.g. Mayer, col. 58, lines 35-

44);

a processor that uses the summary and a content addressable memory, wherein the packet

is associated with one of the second plurality of CCBs, the processor causing said one of the

second plurality of CCBs to be moved from the DRAM into the SRAM (e.g. Mayer, col. 31,

lines 63-67; col. 32, lines 1-30); and

a mechanism that moves the data portion of the packet from the network interface device

and into a destination accessible by the processing device, the data portion of the packet being

written into the destination without the header portion of the packet being written into the

destination (e.g. Mayer, col. 15, lines 46-52).

Mayer fails to teach the network interface device comprising a processor that uses the

summary and a content addressable memory to determine whether the packet can be processed

via a fast-path by the network interface device as opposed to being processed via a slow-path

using the protocol stack; the data portion of the packet being written without the protocol stack

doing substantial TCP protocol processing on the packet.

However, in a similar art, Kapoor teaches a network communications device which

operates on TCP/IP packets using a network protocol stack (e.g. Kapoor, col. 3, lines 49-51) and

also the ability to avoid, or bypass, the processing of a packet on the TCP (transport) layer of the

protocol stack, and if the packet does not meet the requirements for fast processing, performing

processing at each layer of the protocol stack (e.g. Kapoor, col. 2, lines 33-49; col. 6, lines 7-19;

Fig. 2B; col. 5, lines 36-45).

It would have been obvious to one skilled in the art at the time the invention was made to

combine Kapoor with Mayer for similar reasons as stated above in regards to claim 1.

21.   As per claim 18, Mayer and Kapoor teach the network interface device of claim 17,

further comprising a second processor, wherein the processor and the second processor share the

use of the first plurality of CCBs (e.g. Mayer, col. 2, lines 11-28; col. 107, lines 20-33).

22.   As per claim 19, Mayer and Kapoor teach the network interface device of claim 17,

wherein there is a third plurality of CCBs that are under control of the processing device,

wherein control of a CCB can be passed from the processing device to the network interface

device (e.g. Mayer, col. 31, lines 63-67; col. 32, lines 1-30; col. 107, lines 20-33).

23.   As per claim 20, Mayer and Kapoor teach the network interface device of claim 17,

wherein the means is also performing header checksum validation on the packet (e.g. Mayer,

cyclic redundancy checking, col. 14, lines 10-25).

24.   Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mayer et al. (US

6,233,242, hereinafter Mayer) in view of Kapoor et al. (US 5,682,534, hereinafter Kapoor) as

applied to claim 6 above, and further in view of Radogna et al. (US 5,991,299, hereinafter

Radogna).

25.   As per claim 7, Mayer and Kapoor teach the method of claim 6, but fail to teach the

method wherein the specialized hardware comprises a sequencer.

However, in a similar art, Radogna teaches a network communication system that is able

to accelerate packet header protocol processing, including the use of a sequencer (e.g. Radogna,

col. 2, lines 15-28).

It would have been obvious to one skilled in the art at the time the invention was made to

combine Radogna with Mayer and Kapoor because of the advantages of using a sequencer to

perform specific network processing tasks. Additional, specialized hardware, such as a

sequencer to assist the central processing unit in handling simple, redundant tasks that need to be

completed on every incoming and/or outgoing packet. This can greatly reduce processing time

since the CPU is not overloaded with menial tasks and is available to handle more complex

processes faster and more efficiently. Processing and transferring a packet through a network

faster and more efficiently is beneficial in any computer network.

Conclusion

Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Eric Kuiper whose telephone number is (571) 272-0953. The

examiner can normally be reached on Monday through Friday, 8:00am to 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, John Follansbee can be reached on (571) 272-3964. The fax phone number for the

organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent

Application Information Retrieval (PAIR) system. Status information for published applications

may be obtained from either Private PAIR or Public PAIR. Status information for unpublished

applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR

system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Eric Kuiper
27 January 2006

JOHN FOLLANSBEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100